

PATENT APPLICATION

Sheet 1 of 2

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200310231-1

APPLICATION NO.

101735, 849

CONFIRMATION NO.

APPLICANT

Herbert R. KOLK et al.

FILING DATE

Herewith

GROUP

2825

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A				
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

NMD	1Q	Lesley POLKA et al., "Package-Level Interconnect Design for Optimum Electrical Performance," Intel Technology Journal Q3, 2000, pp. 1-17.
NMD	1R	George A. Riley, "Picking Your Flipchip: A Comparison of Flipchip Methods and Benefit," 6 pp. [online] http://www.flipchips.com/SMErev01.htm , Third Quarter 2000, printout date 10/13/2003
NMD	1S	"Calculating the Number of Bumps Needed," 15 pp., printout date 10/13/2003 [online] http://www.artwork.com .

EXAMINER

DATE CONSIDERED

08/28/06

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Sheet 2 of 2

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200310231-1

APPLICATION NO.

10/735,549

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APPLICANT

Herb rt R. KOLK et al.

FILING DATE

Herewith

GROUP

285

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A				
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	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

WMD	1Q	"Die-Bump Designer Suite," CAD Design Software, 4 pp. Date unavailable.
	1R	
	1S	
EXAMINER		DATE CONSIDERED